VARIABLE REFERENCE FREQUENCY TRACKING OF SECOND ORDER VOLTAGE SWITCHED CP-PLL

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ABSTRACT

The charge-pump phase locked loop (CP-PLL) is widely utilized integrated circuit for different applications in communication for frequency generations and tracking. The linear models are not applicable to explore the system dynamics when a variable reference frequency is applied to the system, because of their limited validity in the locked state (i.e. for small phase variations). However the discrete-time non-linear models are advantageous over linear model in characterizing the model behavior when the CP-PLL is initially acquiring the lock on to phase of the reference signal. In this paper, the non-constant reference frequency is applied to both voltage and current switched CP-PLL systems using the event driven technique. The weakly damped dynamics of the voltage switched system limits its performance while tracking the ramping reference frequency due to its varying pumping current characteristics.

Keywords: ***Phase-locked loop, Phase and frequency detector, voltage switched charge-pump. Event driven model, ramping frequency.***

1. INTRODUCTION

The charge-pump phase locked Loop (CP-PLL) is the main subsystem utilized in various applications in wireless communications to industrial electronics (Gardner, 1980; Best, 1984; Margaris, et al, 1985; Ehsan, et al 2012; Weigand, et al, 2011, Brain, et al 1996). The CP-PLL is basically a negative feedback system used to synchronize two signal sources in frequency and phase. The phase detecting unit compares two incoming signal at it inputs (one coming from the reference and other is feedback signal) and detects the phase misalignment in the digital form. The charge-pump (CP) circuit translates the logical outputs of phase detector, encode the phase error signal into a corresponding current or voltage output. Then it is applied to the loop filter (LF) to remove the high order frequency contained in detector signal $\upsilon_{\mathrm{d}}(t)$, and produces a quasi-dc signal which tunes the frequency of the voltage controlled oscillator (VCO).

The CP-PLL has major role in frequency synthesis, a feedback divider depending on the requirement of system (integer or fractional) is implemented in the feedback loop, divides the loop in high and low frequency parts. The current switched charge-pump (CSCP) produces ideally a balanced pump current $i_{\mathrm{P}}(t)$ while speeding up and slowing down the loop dynamics. Many comer-cially CP-PLL ICs (like 4046) incorporate a voltage switched charge pump (VSCP), since the design of such circuit is simple. However including a VSCP enhance the complexity in the dynamical behavior due to the variation

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in the pump current (Gardner, 1980; Best, 1984; Margaris, et al, 1985; Ehsan, et al 2012). To study these effect while non-linear acquisition and locking regions, it requires a systematic approach. Mixed-mode nature of the CP-PLL cannot be explored using any general theory (Christian, et al, 1999 ; Brain, et al 1996).

To characterize the system level behavior different modeling approaches of the CP-PLL exist, e.g. linear s-domain and z-domain models, and discrete time non-linear models (Ehsan, et al 2012 ; Wiegand, et al 2011; Christian, et al, 1997 ; Christian, et al, 1999 ; Paemal, 1994). Linear models are limited to the locked state of the CP-PLL however discrete-time non-linear event driven models are more powerful for the institutive designs, characterization and analysis. In this paper, the second order voltage switched CP-PLL is subjected to the variable reference frequency and it tracking behavior is compared to current switched CP-PLL.

Section II focus on the architecture of CP-PLL system. Event driven modeling in described in the section III. Numerical method is given in section IV. Section V discuss the reference ramping and the simulation result for both architectures of the PLL. Section V summerises the conclusions.

II. ARCHITECTURE

The system level components arranged in the loop are representing the basic architecture of the CP-PLL as shown in Fig.1.

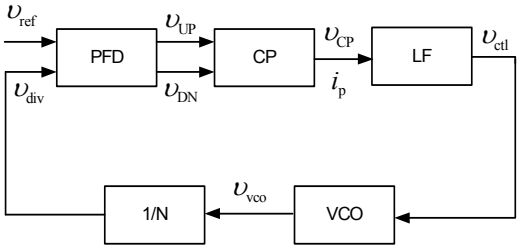

Figure.1: Basic architecture of the CP-PLL.

Phase and Frequency Detector (PFD): The PFD is a digital phase detector which compares the two incoming signals and generates a digital output to command the charge-pump circuit (Best, 1984; Paemal, 1994, Brain, et al, 1996).

Charge-Pump (CP): The CP circuit is controlled by the edge sensitive phase detector circuit and it translates the phase error signal of the PFD into an appropriate analog signal. The charge pumped or removed is proportional the pulse width of the phase error **(**Gardner, 1980; Best, 1984; Margaris, et al, 1985; Ehsan, et al 2012; Christian, et al, 1997; Christian, et al, 1999). The voltage switched charge-pump (VSCP) provides supply voltage to the loop filter, which results in non-constant pump current for three states of the PFD. The VSCP is easier to design than a constant current charge-pump (Best, 1984, Margaris, et al, 1985). However it adds a non-linear characteristic in the pumped current to and from the loop filter (Best, 1984; Margaris, et al, 1985, Ehsan, et al, 2012).

Loop Filter (LF): The LF integrates the pump current to set an average frequency. It is used to smooth the detected signal and suppresses the higher order harmonics in the CP-PFD output signal and passes the low order harmonics only (Gardner, 1980; Best, 1984; Margaris, et al, 1985; Ehsan, et al 2012; Christian, et al, 1997;). The linear, time-invariant differential equation of the lead-lag loop filter is represented as

$$\sum \mathrm{LF}: \begin{cases} \dot{x}(t) = \mathrm{A}\,x(t) + \mathrm{B}\,\upsilon_{\mathrm{d}}(t) \\ \upsilon_{\mathrm{ctl}}(t) = \mathrm{C}^{T} x(t) + \mathrm{D}\,\upsilon_{\mathrm{d}}(t) \end{cases} \tag{1}$$

Voltage Controlled Oscillator (VCO): The VCO is the heart of PLL systems that outputs an oscillating signal with a frequency proportional to the quasi-dc voltage $\upsilon_{\mathrm{ctl}}(t)$ applied to its control node ((Christian, et al, 1997; Paemal, 1994). VCO tuning characteristics are usually represented in a nonlinear curve. However when PLL is locked, $\upsilon_{\mathrm{ctl}}(t)$ varies around a small region and the VCO frequency is represented as

$$\omega_{\mathrm{vco}}\left(\upsilon_{\mathrm{ctl}}(t)\right) = K_{\mathrm{v},\omega}\upsilon_{\mathrm{ctl}}(t) + \omega_{\mathrm{v}\phi} \tag{2}$$

ω_{vco} is angular frequency of the VCO.

$K_{\mathrm{v},\omega}$ is the gain (in rad/sec/V).

$\omega_{\mathrm{v}\varphi}$ is the free running angular frequency.

1/N: The frequency divider is implemented in the feedback loop (Fig.1) in order to perform frequency synthesis function (Christian, et al, 1997; Paemal 1994, Brain, et al 1996). Depending on the requirement the divider can be integer or fractional. Following frequency is generated from the VCO in when the PLL is in the steady state:

$$f_{\mathrm{ref}} = \frac{f_{\mathrm{vco}}}{N} \Rightarrow f_{\mathrm{vco}} = N \bullet f_{\mathrm{ref}} \tag{3}$$

III. EVENT DRIVEN MODELING

The Event Driven technique is based on calculating the commutation instant of two incoming signal. The time point at which effective edge of the signal triggers the PFD is taken into account (see Fig.2). Depending on the calculated time instant phase of the reference and feedback signal is calculated (Ehsan, et al, 2012; Christian, et al, 1997; Christian, et al, 1999). For that, the

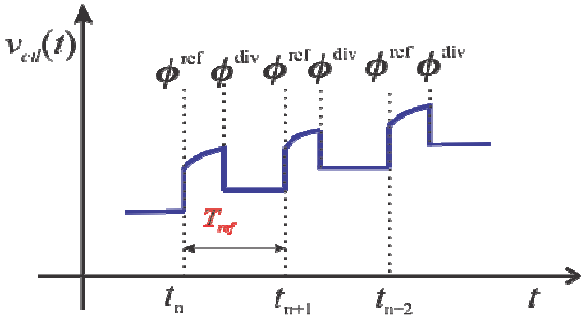

Figure 2: Event-Driven Technique.

non-linear discrete-time event driven phase equations

$$\phi^{\text{ref}}(t_{n+1}) = \phi^{\text{ref}}(t_n) + \int_{t_n}^{t_{n+1}^{\text{ref}}} \omega_{\text{ref}}(t')\,dt' \tag{4}$$

$$\phi^{\text{div}} = \phi^{\text{div}}(t_n) + \int_{t_n}^{t_{n+1}^{\text{div}}} \omega_{\text{div}} \upsilon_{\text{ctl}}(t')\,dt' \tag{5}$$

of respectively the reference and the divider signals have to be solved:

t_{n+1}^{ref} is the solution of $\varphi_{\text{ref}}(t_{n+1}^{\text{ref}}) = 2\pi$ (6.a)

t_{n+1}^{div} is the solution of $\varphi_{\text{div}}(t_{n+1}^{\text{div}}) = 2\pi$ (6.b)

- t_{n+1}^{ref} is the falling edge of the reference signal.
- t_{n+1}^{div} is the falling edge of the divider signal.

The effective falling edge is the one first occurring at:

$$t_{n+1} = \min(t_{n+1}^{\text{div}}, t_{n+1}^{\text{ref}}) \tag{7}$$

Assuming a constant or a non-constant (i.e. ramp) reference signal (see in Fig.3), (5.a) leads to a simple analytical solution for t_{n+1}^{ref}.

However the divider phase equation (5.b) for the voltage switched CP-PLL (VSCP-PLL) is a transcendental expression and t_{n+1}^{div} has to be calculated using numerical method.

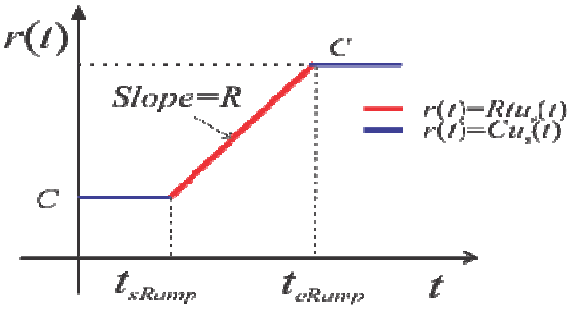

Figure 3: Representing the step $r(t) = Cu_s(t)$ and ramp $r(t) = Rtu_s(t)$ function.

IV. NUMERICAL SOLVING: SECANT METHOD

The secant method is an iterative root finding numerical method. It requires one function evaluation (e.g. Newton-Raphson method requires two functions) so that if the algorithm converges than it is even fast than other methods.

$$t_1 = t_2 - \frac{\phi^{\text{div}}(t_2)(t_2 - t_0)}{\phi^{\text{div}}(t_2) - \phi^{\text{div}}(t_0)} \tag{8}$$

To determine the solution $t_1 = t_{n+1}^{\text{div}}$ the algorithm converges to the condition $\varphi^{\text{div}}(t_{n+1}^{\text{div}}) \equiv 2\pi$.

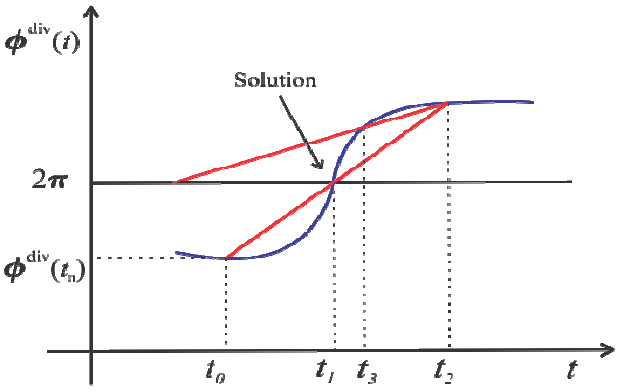

Figure 4: Determination of falling event from divider $t_n = t_{n+1}^{\text{div}}$ using the secant method (this is a simple example of the convergence).

V. VARIABLE REFERENCE FREQUENCY APPLIED TO THE SECOND ORDER VSCP-PLL

Due the versatility of the CP-PLL, it can be applied to track the reference ramp generator (Mush, T, 1998,

Christian, H, 1997). The event driven technique is the most powerful tool to study the dynamic behavior and it allows applying a ramp input frequency to test the tracking ability of the VSCP-PLL (Ehsan et al, 2012, Christian, H, 1999). The input frequency step for the linearly varying ramp must be within lock range of PLL to track it (Best, 1984). Equation (9) represents the inequality that must be satisfied for the slope (β) of the reference frequency ramp to be tracked by the oscillator (Gardner, F, M 1979). This inequality belongs to the constant current system (i.e. current switched CP-PLL). Nevertheless, it is also valid for second order VSCP-PLL using an equivalent model of the CSCP-PLL.

$$\left|\varphi_{\text{err}}^{\text{static}}\right| \le 2\pi \Leftrightarrow \beta \le \frac{K_{\text{v},\omega} I_{\text{p}}}{NC_1} \tag{9}$$

Since the VSCP produces non-constant pump current $i_{\text{p}}(t)$ as a function of electrical load of LF, which limit-- ---the ability of the system when tracking the ramp function of the frequency.

$$i_{\text{p}}(t) = \frac{V_{\text{CP}} - \upsilon_{\text{C1}}(t)}{R_0 + R_1} \tag{10}$$

As soon as the capacitor voltage $\upsilon_{C1}(t)$ approaches V_{CP}, the pump current reaches its minimum.

a. SIMULATION RESULT

The event driven model of the second order CP-PLL is subjected to a reference generator ramp. Here both systems (CSCP-PLL & VSCP-PLL) are considered as shown in Fig. 5. The Fig. 5 is divided in differemt zones A...G.

In zone-A, both systems are showing an erratic behavior before locking to the target frequency (1MHz). Both models are locked and settled in the zone-B. The ramping frequency (1MHz to 3Mhz) is applied in zone-C, the positive frequency ramp starts at 200µs and ends at 433µs and reaches a target frequency of 3MHz. The phase error $\phi_{\text{err}}(t)$ of the VSCP-PLL is not converging to a constant value (unlike CSCP-PLL, which is converging to a constant value) but it is increasing during the ramp tracking period. This is the consequence of week pump current (10). Settling behavior of both systems can be seen in the zone-D, which describes the equivalent behavior of both systems. In the zone-E, it is obvious that, CSCP-PLL is tracking a bit longer ramp inclination of reference frequency with a negative slope, but the VSCP-PLL is *pulled-out* of the lock (circled area in the phase transient) in zone-F, however CSCP-PLL is efficiently tracking in this region. In the zone-G, after unlocking, once again the VSCP-PLL acquires the lock and it is settled. The voltage switched system exhibit the lack of ability in tracking a ramp, whereas similar ramp is completely followed by the CSCP-PLL, on the other hand, CSCP-PLL continues tracking without losing the lock. The phase-plane of the both systems is shown in Fig. 6, which shows that after an erratic region the system is converged to a target frequency, the system settles three times in the steady state.

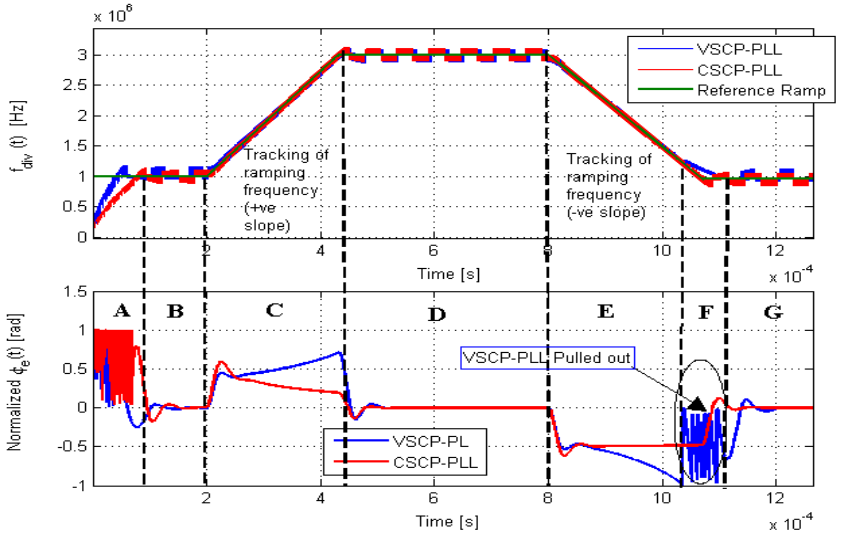

Figure 5: The phase error response of the both CSCP-PLL and VSCP-PLL to two successive reference frequency-ramps.

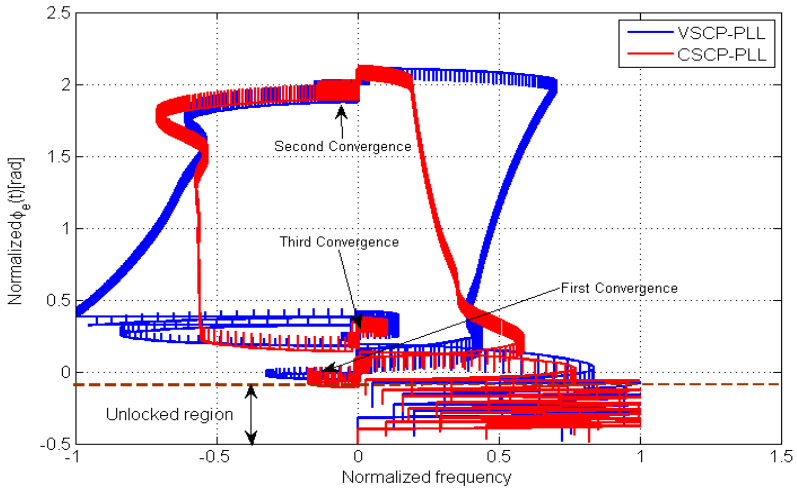

Figure 6: The phase-plane of both CSCP-PLL and VSCP-PLL when tracking two successive reference frequency-ramps.

VI. CONCLUSION

The event driven model of the voltage switched CP-PLL was subjected to the variable reference frequency. It shows that week dynamics due the non-constant pump current influences the dynamical behavior of the second order VSCP-PLL. This peculiarity limits its performance in tracking a ramping reference frequency. On other hand the CSCP-PLL has strong dynamics due to its ideally constant pump currents and it can track a variable frequency within the inequality condition described. The designer must be careful to pump current conditions to meet a desired accuracy for frequency tracking applications.

REFERENCES

[1] Gardner F. M. (1980), Charge Pump Phase Locked Loop, IEEE Transaction Communications, vol COM-28, No. 11, pp 1849-1858.

[2] Gardner F. M. (1979), Phase Lock Techniques, First edition, Willy

[3] Best R. E. (1984) Phase Locked Loop Design, Simulation and Applications, McGra Hill.

[4] Margaris I., N. and Petridis V (1985) Voltage Pump Phase-Locked Loops, IEEE Transactions On Industrial Electronics, vol. IE-32, No.1.

[5] Ehsan Ali, C Wiegand, C Hangmann, C Hedayat and Dieter Kraus (2012) Event Driven Simulation of the Second Order Voltage Operated CP-PLL, SAME conference, 2-3, Nice France.

[6] Wiegand C, Hangmann C, Hedayat C, and Hilleringmann U (2011) Modaling and Simulation of Arbitrary Ordered Nonlinear Charge-Pump Phase-Locked Loops, Semi-conducteur Conference Dresden.

[7] Christian D. Hedayat, Ahmed Hachem, Yves Leduc and Geärar Benbassabt (1997) Level Modeling applied to second order charge-pump PLL circuit, TI Technical Journal.

[8] Christian D. Hedayat, Ahmed Hachem, Yves Leduc and Geärar Benbassabt. (1999) Modeling & Characterization of the 3rd Order Charge-Pump PLL: a Fully Event-driven Approach, Analog Integrated Circuits and Signal processing 19, pp 25-45.

[9] Paemal, M. V., (1994) Analysis of a Charge-Pump PLL: New Model, IEEE Transactions on Communication Vol. 42 No. 7.

[10] Brain AA Antao, Fathey Mel-Turky and Robert H Leonowich (1996) Behavioral Modeling Phased Locked Loop for Mixed- Mode Simulation, Analog Integrated Circuits and Signal Processing, Kluwer Academic Publishers, Boston. Manufactured in The Netherlands.

[11] Musch, T., I. Rolfes, B. Schiek, (1998): A Highly Linear Frequency Ramp Generator Based On a Fractional Divider Phase-Locked-Loop, Ruhr-Universitat Bochum, Institut fur Hochfrequenztechnik Universitats straße 150, D-44780 Bochum, Germany Precision Electromagnetic Measurements Digest, 199.